IN THE CLAIMS:

1. (Currently Amended) An integrated circuit device comprising:

a semiconductor substrate;

a metallization interconnect system overlying the semiconductor substrate, the metallization interconnect system including multiple first interconnect structures located within a dielectric layer;

a bond pad level comprising a contact pad overlying the metallization interconnect system, the contact pad configured for connection external to the device;

a second interconnect structure connected to the contact pad, wherein a portion of the second interconnect structure is disposed in the bond pad level, the second interconnect structure being in physical contact with the multiple first interconnect structures located within the dielectric layer; and

a passivation layer overlying at least a portion of the bond pad level.

2. (Previously Presented) The integrated circuit device of claim 1 wherein a material of the metallization interconnect system comprises copper.

3. (Previously Presented) The integrated circuit device of claim 1 wherein a material of the contact pad comprises aluminum.

4. (Previously Presented) The integrated circuit device of claim 1 wherein the contact pad

is configured for connection external to the device by a bond wire attached thereto.

5. (Previously Presented) The integrated circuit device of claim 1 wherein contact pad is configured for connection external to the device by a solder bump attached thereto.

6. (Previously Presented) The integrated circuit device of claim 1 wherein a material of the metallization interconnect system comprises copper and the contact pad comprises aluminum, further comprising a barrier material between the copper and the aluminum in regions where the second interconnect structure is in physical contact with the multiple first interconnect structures located within the dielectric layer .

7. (Canceled)

8. (Previously Presented) The integrated circuit device of claim 1 wherein the metallization interconnect system further comprises substantially horizontal conductive runners and substantially vertical conductive vias interconnecting overlying and underlying conductive runners.

9. (Previously Presented) The integrated circuit device of claim 8 wherein a material of the substantially horizontal conductive runners and the substantially vertical conductive vias comprises copper.

10. (Previously Presented) The integrated circuit device of claim 1 further comprising a passivation layer disposed between the second interconnect structure and the dielectric layer.

Claim 11 (Canceled)

12. (Currently Amended) An integrated circuit device comprising:

a metallization interconnect system located over a substrate, the metallization interconnect system including multiple first interconnect structures located within a dielectric layer;

a plurality of contact pads disposed over the metallization interconnect system, one or more of the plurality of contact pads configured for connection external to the device; ~~and~~

a second interconnect structure coplanar with at least one of the plurality of contact pads and electrically connected thereto, the second interconnect structure comprising a plurality of conductive elements physically contacting the multiple first interconnect structures; and

a passivation layer overlying at least a portion of the second interconnect structure.

13. (Previously Presented) The integrated circuit device of claim 12 wherein a material of the metallization interconnect system comprises copper.

14. (Previously Presented) The integrated circuit device of claim 12 wherein a material of

the contact pads and the second interconnect structure comprises aluminum.

15. (Previously Presented) The integrated circuit device of claim 12 wherein the metallization interconnect system comprises substantially horizontal conductive runners and substantially vertical conductive vias interconnecting overlying and underlying conductive runners.

16. (Previously Presented) The integrated circuit device of claim 15 wherein a material of the substantially horizontal conductive runners and the substantially vertical conductive vias comprises copper.

Claims 17-25 (Canceled)

26. (Previously Amended) The integrated circuit of claim 1 wherein at least a portion of the second interconnect structure is disposed above the contact pad.

27. (Previously Presented) The integrated circuit of Claim 1 wherein the second interconnect structure is a power bus.

28. (Previously Presented) The integrated circuit of Claim 12 wherein the second interconnect structure is a power bus.

29. (New Claim) The integrated circuit of Claim 1 wherein the passivation layer is patterned to protect the second interconnect structure and expose the contact pad.